Q.P. Code:**16EC5703** **R16**

Reg. No. | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

M.Tech I Year I Semester Regular & Supplementary Examinations February 2018

DIGITAL IC DESIGN

(VLSI)

Time: **3** hours Max. Marks: **60**

(Answer all Five Units **5 X 12 =60** Marks)

UNIT-I

1	a.	What is clock skew problem and how is it overcome in domino CMOS circuits?	7M
	b.	Compare the power dissipation of static CMOS and dynamic CMOS	5M
		OR	
2	a.	How does the domino logic solves the problem in dynamic logic?	4M
	b.	Design a static CMOS circuit for XNOR gate.	8M

UNIT-II

3	a.	Explain about different strategies for building low power CMOS gates	6M
	b.	With a neat sketch explain the working of a 4 transistors SRAM	6M
		OR	
4	a.	Give short notes on logical effort?.	5M
	b.	What are the design consideration of a 4 bit SRAM with the help of CMOS logic diagram.	7M

UNIT-III

5	a.	How do we calculate power for BiCMOS and on what parameters the power equation depends on?	8M
	b.	Design NAND gate in BiCMOS logic	4M
		OR	
6	a.	Elaborate about bipolar gate design in detail with neat sketches.	7M
	b.	Explain the concept of BiCMOS inverter	5M

UNIT-IV

7	a.	What are the general observations on the design rules?	6M
	b.	Give short notes on NMOS based design rules.	6M
		OR	
8	a.	Write about: (i) Sheet resistance.	7M
	b.	(ii) Lambda based design rules.	5M

UNIT-V

9	a.	Compare different types of CMOS subsystem shifters	7M
	b.	List the design approach of 4 bit shifter	5M
		OR	
10	a.	How to design the ALU sub-system? Give the process	5M
	b.	Explain in detail about subsystem design process.	7M

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